Version Issues with Xilinx Software in Engineering 163 – Fall 2004

You will need to use the Xilinx ISE software package to program the XC9572XL CPLD's used in labs 3, 4, 5, 7, A, and B and to program the Field Programmable Gate Arrays used in labs C, D, E, and F. There is a problem that downloading files into the hardware must be done with version ISE 6.2 to be compatible with the new XP operating system but the FPGAs must have their code compiled with version ISE 4.2. We have both versions available on the machines in both the lab (Room 196) and the Computing Facility. You have to select the correct version for what you are trying to do and this is somewhat tricky. Here are the basic instructions:

To compile a file for the CPLDs:

1. Run the menu sequence Start/Electrical/Xilinx/Xilinx ISE 6/Run Me First. This selects the ISE 6 version to be run.

2. Use the menu sequence Start/Electrical/Xilinx/Xilinx ISE 6/Project Navigator to start the compiler and follow the instructions in the back of the lab manual to compile your ABEL code into a ".jed" file for downloading.

To download into a CPLD:

1. Run the menu sequence Start/Electrical/Xilinx/Xilinx ISE 6/Run Me First. This selects the ISE 6 version to be run.

2. Use the menu sequence Start/Electrical/Xilinx/Xilinx ISE 6/Accessories/iMPACT to start the downloading tool. Follow the instructions in the back of the lab manual to download into the CPLD board. Please remember not to power up a board from your prototype before it is programmed. Use the power cable on each supply to power it with no input or output connections first.

To compile into an FPGA:

1. Run the menu sequence Start/Electrical/Xilinx/Xilinx ISE 4/Run Me First. This selects the ISE 4 version to be run.

2. Use the menu sequence Start/Electrical/Xilinx/Xilinx ISE 4/Project Navigator to start the compiler and follow the instructions in the back of the lab manual to compile your schematic or VHDL code into a ".bit" file for downloading.

To download into an FPGA:

1. Run the menu sequence Start/Electrical/Xilinx/Xilinx ISE 6/Run Me First. This selects the ISE 6 version to be run. Note: you must use version six for all downloads but FPGA wiring must be compiled in version 4. The Run Me First files select between the two versions.

2. Use the menu sequence Start/Electrical/Xilinx/Xilinx ISE 6/Accessories/iMPACT to start the downloading tool. Follow the instructions in the back of the lab manual to download into the CPLD board. You use the bit serial mode rather than JTAG mode for this download.